Power Electronics and Drives

All-Bootstrap Gate-Driver Supply System for a High-Voltage-Gain Resonant DC-DC Converter with Seven Switches

Research Article

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Abstract: This paper presents the concept and implementation of an electronic system for a switched-capacitor DC-DC converter with high voltage gain. The converter consists of seven switches, five of which being controlled like high-side type. This paper presents a non-typical bootstrap-based gate-driver system so that the converter can run using a single voltage source. The converter requires a special switching pattern to drive seven switches in a steady state and also during the start-up of the converter and the regulation of the output voltage. Therefore, an FPGA-based digital control system is used with various switching algorithms and protection functions implemented. The presented converter is an autonomic device that taps the energy from the main input. Therefore, the electronic system of the converter is equipped with a self-supply system with a wide range of the input voltage. The parameters of the converter such as voltage gain, voltages and power ranges can be scalable for prospective applications with the proposed control system.

Keywords: FPGA • DC-DC converter • digital control • gate-driver circuit

1. Introduction

In power electronics, switched-capacitor (SC) converters can be utilised for high-voltage-gain systems or for the applications where inductiveless design is beneficial, e.g., due to a high temperature of operation. Various types of topologies are presented in literature, such as those in (loinovici, 2001), or (Tang et al., 2011), or more (Li et al., 2018; Maalandish et al., 2018; Salvador et al., 2018; Stala et al., 2019a; Wu et al., 2015; Xiong and Tan, 2015). Many of them contain resonant circuits that allow for zero current switching (ZCS), thus limiting switching losses.

This type of energy conversion often requires the application of a large number of semiconductor switches and non-typical switching patterns. Gate-driver circuits can be complex, unless an effective supply method is used. In some switched-capacitor voltage multipliers (SCVMs), such as presented in (Callegaro et al., 2019; Eguchi et al., 2003; Hwu et al., 2013), a bootstrap-type supply system for all high-side switches is used and demonstrated.

The resonant converter presented in this paper (Figure 1) and described in (Stala et al., Patent; Stala et al., 2019b) is based on the SCVM topology, but it is more complex since it supplies two output capacitors connected in series. Its voltage gain is nearly doubled when compared to that of a classic SCVM converter (Penczek et al., 2017), and in case of a three–cell system, the gain is close to G = 7. However, the bootstrap method for the gate drivers is still possible in this converter (Figure 1), which is an important novel contribution presented in this paper.

It must be noted that a non-typical switching pattern should be often generated for a large number of switches for the proper operation of an SC converter and its bootstrap circuits. In our proposed system, a digital FPGA-based controller is used. The steady-state switching, start-up of the converter as well as protection functions can be achieved using a controller with an Intel FPGA Max10 chip.

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One of the prospective areas of the applications of high-voltage-gain converters, such as the proposed SC circuit (Figure 1) are photovoltaic systems. A self-supply of the electronic parts from the main input is a beneficial solution in such a case. In the analysed system, the circuit is designed in a way to deliver stable on-board voltage immediately once the input voltage achieves a desired level.

This paper is organised as follows: Section 2 presents the general concept of the operation of the converter, and Section 3 demonstrates the concept of the bootstrap circuits. In Section 4, the converter's operation with a decreased voltage gain is discussed. Section 5 describes the experimental setup, the switching pattern, and the FPGA-based controller. Moreover, it shows the concept of the self-supply system, and presents the experimental results related to the designed electronic functional blocks.

2. Basic Operation of the Converter and Its Switching Pattern

The basic concept of the converter is presented in (Stala et al., Patent) and (Stala et al., 2019b). Furthermore, various simulation and experimental results related to the operation of the converter are presented by (Stala et al., 2019b).

During the steady state, the proposed converter operates in four consecutive stages in every switching period which is confirmed and presented in (Stala et al., 2019b):

- stage 1: all the switched capacitors are charging,
- stage 2: all the switched capacitors are discharging to the upper output capacitor C_{outt},
- stage 3: two first switched capacitors (C_1 and C_2) are charging,
- stage 4: two first switched capacitors (C_1 and C_2) are discharging to the lower output capacitor C_{outp} .

Based on the results presented in (Stala et al., 2019b), it is concluded that the converter achieves voltage gain G = 7. Typically for SC converters, the voltage gain decreases as the load increases and, for 450 W, it approaches G = 6.5 at $U_{in} = 50$ V. The peak efficiency (91.91%) of the converter operating with $U_{in} = 50$ V was achieved at $P_{out} = 305$ W.

Table 1 presents the switching patterns required for the operation concept. The converter operates using four stages of switching in each switching period.



Fig. 1. High-voltage-gain DC-DC converter (Stala et al., 2019b)

Table 1. Four-stage switching pattern for the voltage gain G=7

	S1	S2	S3	S4	S5	S6	Saux	Action
Stage 1	1	0	1	0	1	0	1	Capacitors C_1 , C_2 , C_3 are charging
Stage 2	0	1	0	1	0	1	1	Capacitor C _{out1} is charging
Stage 3	1	0	1	0	0	0	0	Capacitors C_1 , C_2 are charging
Stage 4	0	1	0	1	1	1	0	Capacitor C_{out2} is charging

3. Gate-driver Supply System

The converter consists of seven switches. The supply network of the gate drivers is presented in Figure 2. Three transistors *S*1, *S*3 and *S*aux are low-side switches connected to the supply source. Three switches, *S*2, *S*4 and *S*5, may have bootstrap-type supply containing the corresponding low-side switches (Figure 2 and Table 2). The high-side switch *S*6 uses energy from the capacitor that is charging in the bootstrap circuit composed of two power transistors *S*5 and *S*aux. This is feasible because transistors *S*5 and *S*aux are turned on simultaneously, i.e., during the charging of the switched capacitor *C*3. This case is presented in Figure 3 that shows the current paths in the bootstrap circuits. The remaining steady-state stages of operation are not complicated from the gate-driver supply aspect. Further, the converter configuration in all the steady-state stages of operation is presented in (Stala et al., Patent) and (Stala et al., 2019b).



Fig. 2. Practical solution of the SC converter with bootstrap gate-driver supply network for seven switches

Table 2. The bootstrap capacitor's charging in the switching stages 1 and 3

	S1	S2	S3	S4	S5	S6	Saux	Bootstrap circuit conditions
Stage 1	1	0	1	0	1	0	1	All the bootstrap capacitors are charging
Stage 3	1	0	1	0	0	0	0	The bootstrap capacitors in gate drivers of S2 and S4 are charging

4. Operation with a Decreased Voltage Gain

According to the algorithms presented in (Stala et al., 2019a) and (Penczek et al., 2017), it is possible for the converter to operate with various voltage gains (*G*). The principle is based on the operation with a various number of the active SC branches. Further, the branches with the switched capacitors C_1 and C_2 can be bypassed for a decreased voltage gain. The operation with one switched capacitor determines the minimum limit of voltage on the output capacitors, and $U_{outmin} = 2U_{in}$ and U_{outmin} . Therefore, the voltage gain regulation in the range $G = \{4, 5, 6\}$ is reasonable. The bootstrap circuits operate correctly at each voltage gain level presented in Table 3 since switches Saux, and Saux together with S5 are activated in each case.



Fig. 3. The current paths in bootstrap circuits at stage1 of the switching period

Table 3.	Voltage	gain (G)	and	bootstrap	supply	operation
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G		S1	S2	S3	S4	S5	S6	Saux	Average output voltages
6	Stage 1	0	0	1	0	1	0	1	$U_{\rm out1} = U_{\rm in} + U_{\rm C2} + U_{\rm C3} = 3U_{\rm in}$
	Stage 2	0	0	0	1	0	1	1	$U_{\text{out2}} = U_{\text{in}} + U_{\text{C1}} + U_{\text{C2}} = 3U_{\text{in}}$
	Stage 3	1	0	1	0	0	0	0	$U_{out} = 00_{in}$ where U_{o} is the average value of voltage across
	Stage 4	0	1	0	1	1	1	0	the given capacitor
5	Stage 1	0	0	1	0	1	0	1	
	Stage 2	0	0	0	1	0	1	1	$U_{\text{out1}} = U_{\text{in}} + U_{C2} + U_{C3} = 3U_{\text{in}}$
	Stage 3	0	0	1	0	0	0	0	$U_{\text{out2}} = 5U_{\text{in}} + U_{C2} = 2U_{\text{in}}$
	Stage 4	0	0	0	1	1	1	0	out in
	Stage 1	0	0	0	0	1	0	1	
4	Stage 2	0	0	0	0	0	1	1	$U_{\text{out1}} = U_{\text{in}} + U_{C3} = 2U_{\text{in}}$
	Stage 3	0	0	1	0	0	0	0	$U_{out2} = U_{in} + U_{C2} = 2U_{in}$ $U_{in} = 4U_{in}$
	Stage 4	0	0	0	1	1	1	0	- out - in

5. Experimental Setup and Results

The experimental setup of the complete converter is presented in Figure 4. The converter contains the following parts:

- the main PCB with the power circuit, electronic self-supply system and gate-driver supply network,
- the FPGA-based controller on the external PCB attached to a dedicated 40-pin slot,
- the heat sink on the bottom side of the main board and
- the input and output capacitors.

The converter's parameters are presented in Table 4.

5.1. The switching pattern

Figure 5 shows the waveforms of the gate signals of transistors Saux, S5 and S6. From these waveforms, it is observed that the gate-driver voltage is maintained correctly for the high-side transistors S5 and S6.



Fig. 4. The complete DC-DC high-voltage-gain converter

Table 4. Parameters of	of the	converte
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Input/Output voltage	50 V/350 V
Resonant frequency	$f_0 = 122.06 \text{ kHz}$
Operating frequency	$f_{\rm S} = 58 \text{ kHz}$
SC capacitance	470 nF+100 nF (KEMET R76 series)
Resonant inductances	Planar chokes: 3F36 Ferrite E18 Core, $d = 0.5$ mm, 6 turns in PCB, ($L = 2.97 \mu$ H, $R_{_{ESR}} = 50 \text{ m}\Omega$ @120 kHz)
Transistors	BSC160N15NS5 ($V_{\rm DS}$ = 150 V, $R_{\rm DSon}$ = 16 m Ω), RFS4229PbF ($V_{\rm DS}$ = 300 V, $R_{\rm DSon}$ = 42 m Ω)
Diodes	VB60170G ($l_{\rm F}$ = 2 × 30 A, $V_{\rm RRM}$ = 170 V, $V_{\rm F}$ = 0.87 V) STTH30L06 ($l_{\rm F}$ = 30 A, $V_{\rm RRM}$ = 600 V, $V_{\rm F}$ = 1 V)



Fig. 5. Experimental waveforms of gate signals of transistors Saux (1), S5 (3) and S6 (2)

5.2. FPGA-based controller

Figure 6 presents the diagram and a photograph of the FPGA-based controller. The circuit contains Intel MAX10 10M16SAE144C8G device, other components responsible for output voltage measurement and signal conditioning.

Figure 7 shows the waveforms of control signals generated for all the switches in the FPGA-based generator. This switching pattern is used for a steady-state operation of the converter at G = 7 while in other cases, the controller generates switching patterns for the starting procedure or output voltage regulation, as in (Penczek et al., 2017), and for the algorithms of protection.

Experimental waveforms that confirm the operation of the converter are depicted in Figure 8.

5.3. Self-supply of the on-board components

An autonomous power supply system is implemented to supply the MOSFET drivers and the auxiliary circuits (control board, analogue circuits, etc.). The system is powered by the input voltage of the converter (e.g., solar panel voltage); therefore, no other additional energy source is required.



Fig. 6. Implementation of the FPGA-based controller



Fig. 7. The switching pattern used for a steady state operation. Waveforms of control signals produced for all the switches in FPGA-based generator (Intel Quartus II/Signal-tap Logic Analyzer Software)



Fig. 8. Experimental steady state waveforms of input current (i_{in}) , current of diode D3 (i_{D3}) , voltage on capacitor $C_1 (u_{C1})$ and voltage on capacitor $C_3 (u_{C3})$; $P_{out} = 300 \text{ W}$



Fig. 9. (a) Diagram of the self-supply system, (b) Experimental waveforms of the self-supply system: the power supply voltage u_{in} (1), the output voltage of the gate drivers' supply converter VCC (+15V) (2), and the stabilised voltage +5V (3)

Figure 9 shows the diagram and waveforms of the self-supply system. After the power supply voltage has reached the value of about 15 V, the required output voltages are produced. The whole procedure takes about 20 ms.

6. Conclusions

In this paper, the proposed system of a high-voltage-gain converter is discussed and its implementation is also demonstrated. The converter operates on the principle of switched-capacitor voltage multipliers, and its unique topology allows for a reduction in the number of switches. The correctness of its operation has been tested using the experimental setup presented. The setup results in a solution that can be used to build a prototype and final product.

The paper significantly enhances the results related to the analysed converter presented in (Stala et al., 2019b), where the steady state operation, voltage gain and efficiency results are presented. Further, in this paper, various aspects of the practical implementation are demonstrated.

The converter utilises an FPGA-based digital control system implemented with various switching algorithms and protection functions. It is a flexible solution; therefore, the control system functions can be easily modified.

The important contribution of this paper is the application of a non-typical bootstrap-based gate-driver system that allows both the high- and low-side transistors to operate using a single power supply circuit.

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